Application of Mimix Asia's X-Band, 10-Watt Power Amplifier MMIC

(1) Introduction

Advanced X-band radars are based on using active phased-array antennas. Mimix Asia offers the XP1006 as an important building block around which the phased-array can be designed. Shown in Figure 1 is a typical application for the XP1006, and is shown as part of one of many elements included in a phased-array radar antenna. The XP1006 in this application can replace the cascade chain making up the traditional driver and HPA functions.

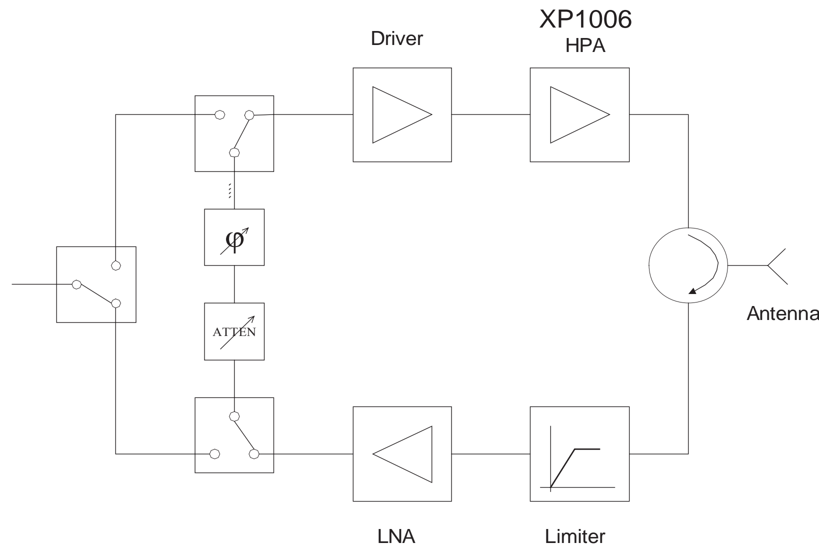

Figure 1: Typical Application, Phase array Antenna Element

The XP1006 is suitable for use in a conventional TR module, or ideally suited in modules based around a highly integrated "Core Chip" which will be shortly offered by Mimix Asia.

Performance criteria of the XP1006 that make it highly desirable for X-band pulsed radar applications are as follows:

- 10W Typical Output Power;
- 21dB of gain in compression;
- more than 25% PAE; and
- more than 25% bandwidth.

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(2) XP1006 Design

The XP1006 is a 3-stage design using a 0.5um GaAs pHEMT process. The MMIC has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either conductive epoxy or solder die attach. Shown in Figure 2a is the layout of the XP1006, and Figure 2b shows the topology.

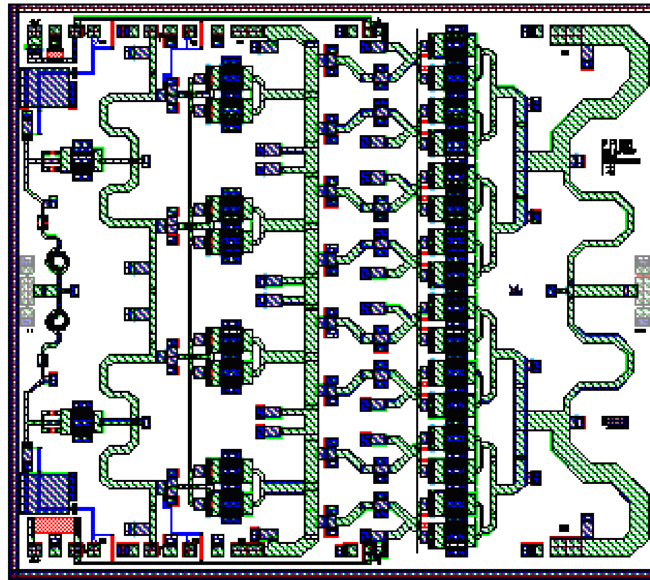

Figure 2a: XP1006 Layout

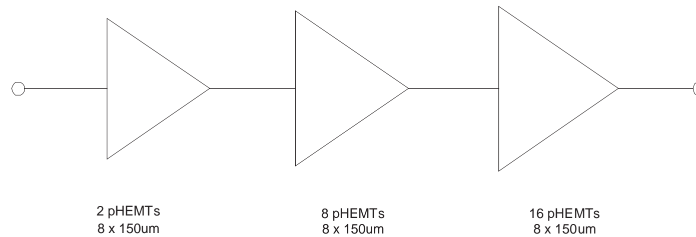

Figure 2a: XP1006 Topology

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The XP1006 on-chip bias circuit provides a convenient and compensated means of gate biasing. A nominal voltage of -5V is applied to the Vgg pad (pad # 2). This voltage is applied to both the gate and source (i.e. Vgs=0V) of a pHEMT which has one gate of width 100µm. A drain current of approximately 30mA is generated as a result, and flows through a 25Ù resistor to GND. The drain voltage of approximately -0.75V is then distributed and used as the gate voltage (Vg) for all pHEMTs on the MMIC. The exact value of Vg can be sensed on pad # 3.

The amount of drain current resulting from tying the bias circuit pHEMT gate to source (Vgs=0), is dependent on the pHEMT V_{TO}. If the pHEMT has higher V_{TO} than nominal, the drain current is reduced and the generated Vg rises. Similarly, if V_{TO} is lower than nominal, the drain current increases, leading to a lower Vg. It is assumed that the V_{TO} (variations in nominal value; variations over temp) of the bias circuit pHEMT is similar to all pHEMTs on the MMIC, hence resulting in “compensated” bias.

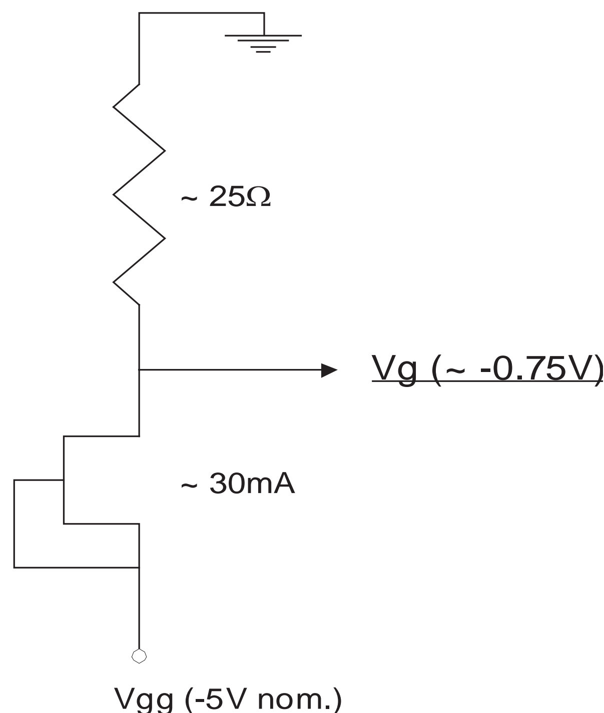

Figure 3 : On-Chip Bias Circuit, V_{TO} Compensated

Two alternative bias points can be used, if more appropriate for the application;

a) Vgg’ (Pad # 18). On-Chip bias circuit (nom. -5V input) but is not V_{TO} compensated
b) Vg (Pad # 17). Biases the On-Chip bias circuit, and allows the gate voltage to be applied directly (e.g. -0.75V)

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(3) Practical Considerations when using the XP1006

Decoupling, Bonding

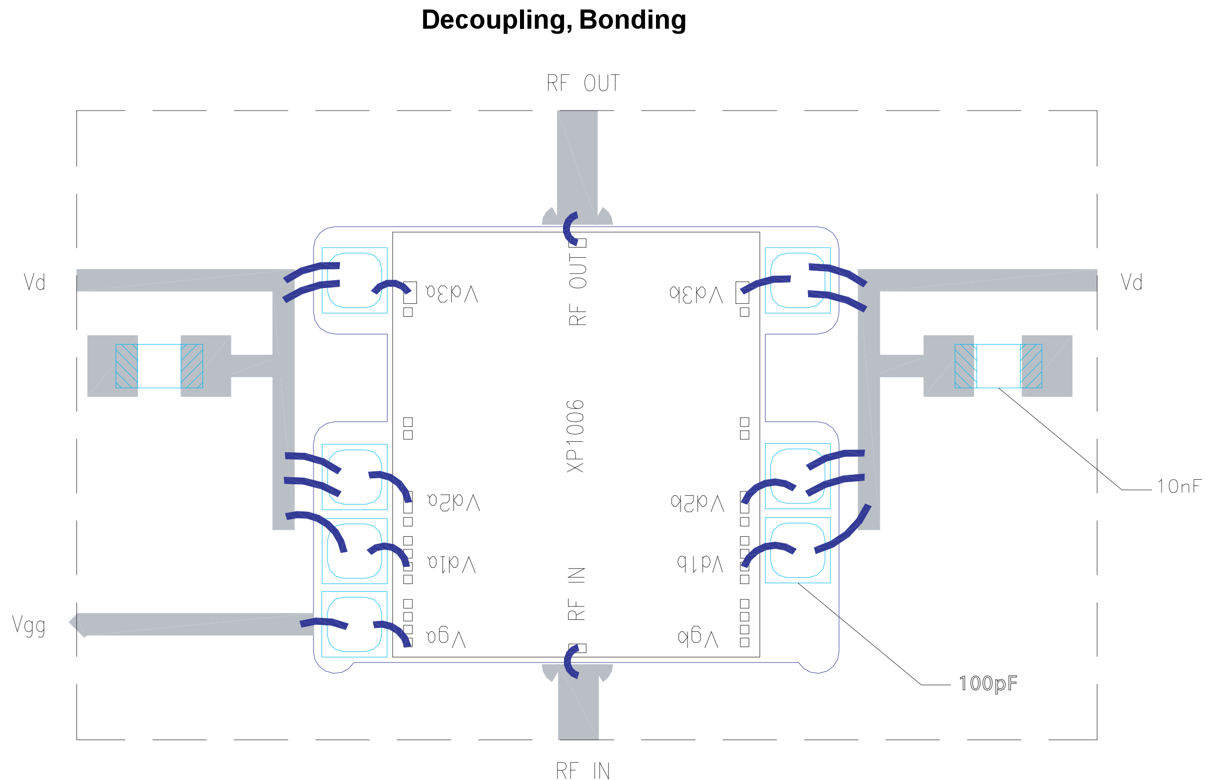

Figure 4: XP1006 Example of Decoupling/Bonding

Notes on Decoupling/Bonding

a) Place 100pF single layer capacitors close to the MMIC as shown in Figure 4
b) Place 10nF single layer or surface mount capacitors close by the 100pF capacitors as shown in Figure 4
c) All drains can be combined on each side, and then the two sides combined at a convenient point away from the MMIC. See Figure 4
d) Ensure bonding wire/ribbon and circuit board traces are substantial enough to handle the current drawn by the MMIC
e) Ensure adequate heat-sinking

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Die Attach

The recommended attach processes are;

(a) Eutectic solder (80%Au, 20%Sn):

a) Reflows at 280°C
b) If used in a vacuum or under a forming gas, soldering can be achieved without use of a chemical flux
c) Exhibits good wettability
d) High yield strength
e) Resistant to creep
f) Corrosion resistant
g) Good thermal conductivity

(b) Thermally Conductive Epoxy

a) E.g. Diemat 6030HK, Tanaka TS3332LD
b) Thermal properties similar to eutectic solder
c) Simple, less specialize process than eutectic die attach
d) Low cost assembly method

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(4) Testing

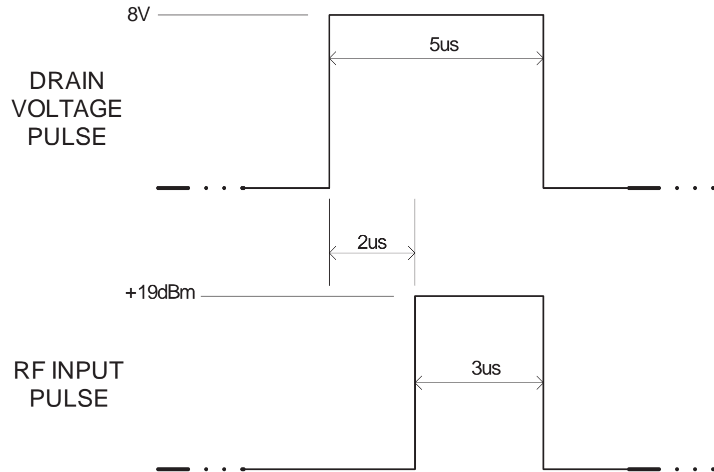
The XP1006 is delivered to customers after having been 100% RF tested, under conditions similar to those of a typical application.

RF/DC Pulse Criteria

DC Pulse Width = 5us

RF Pulse Width = 3us

PRF = 10kHz



Drain Current Monitoring with 0.1V/A (4.2A nom.)

Drain Voltage Monitoring (8V nom.)

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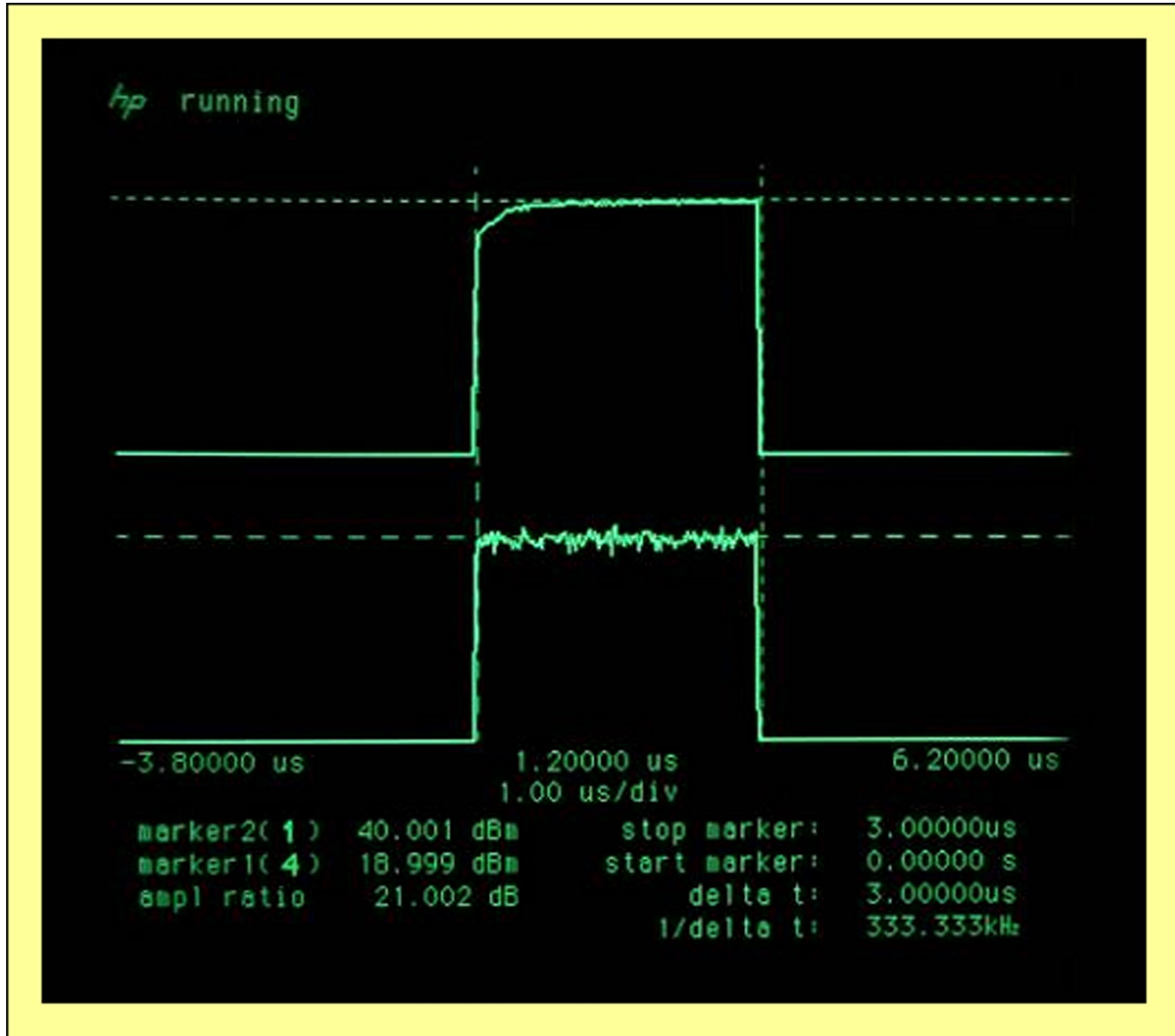

Figure 5: RF Input and Output Pulses (from Peak Power Meter)

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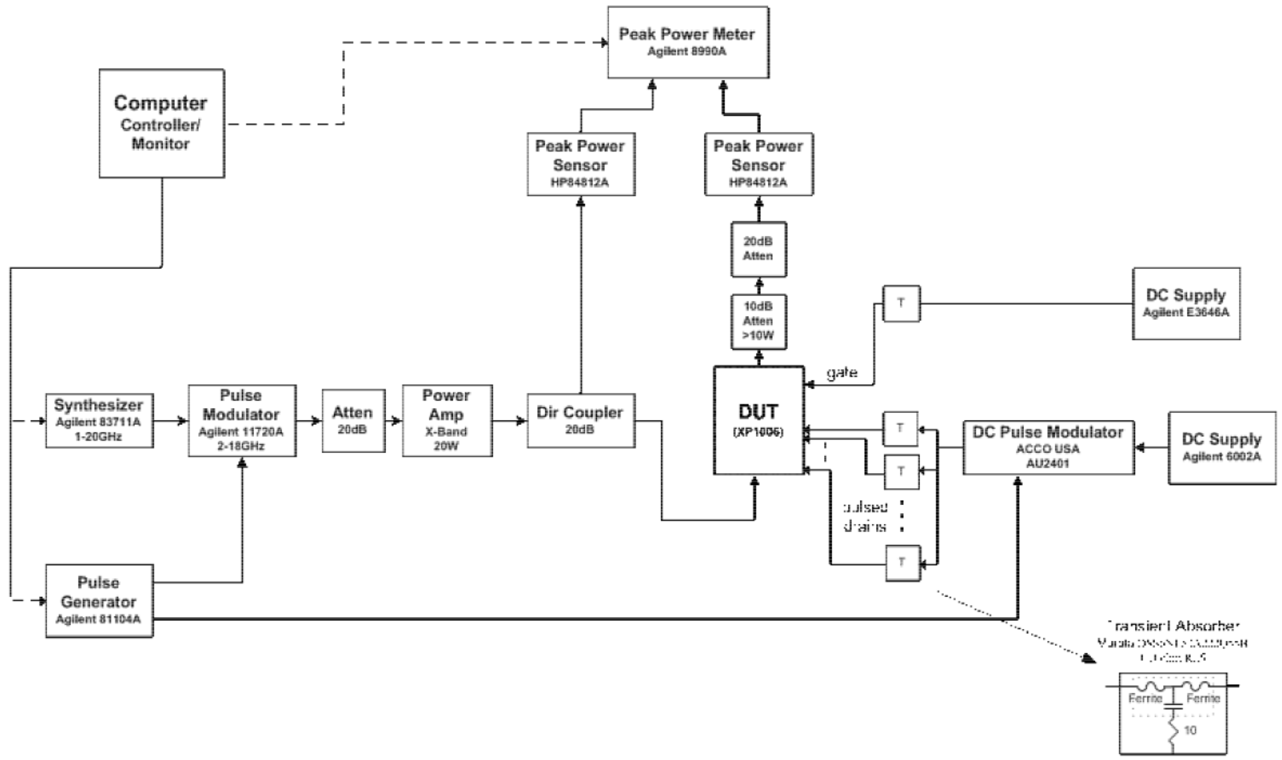

Figure 6: XP1006 Pulsed Measurement Block Diagram

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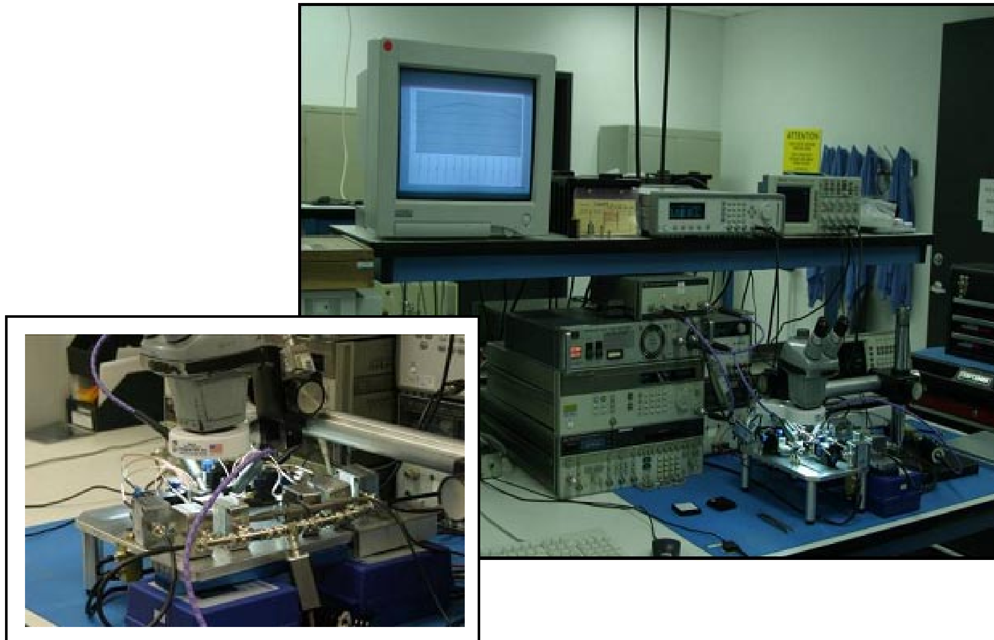

Figure 7: XP1006 Pulsed-mode Qualification

Figure 8: XP1006 Pulsed-mode Production Testing

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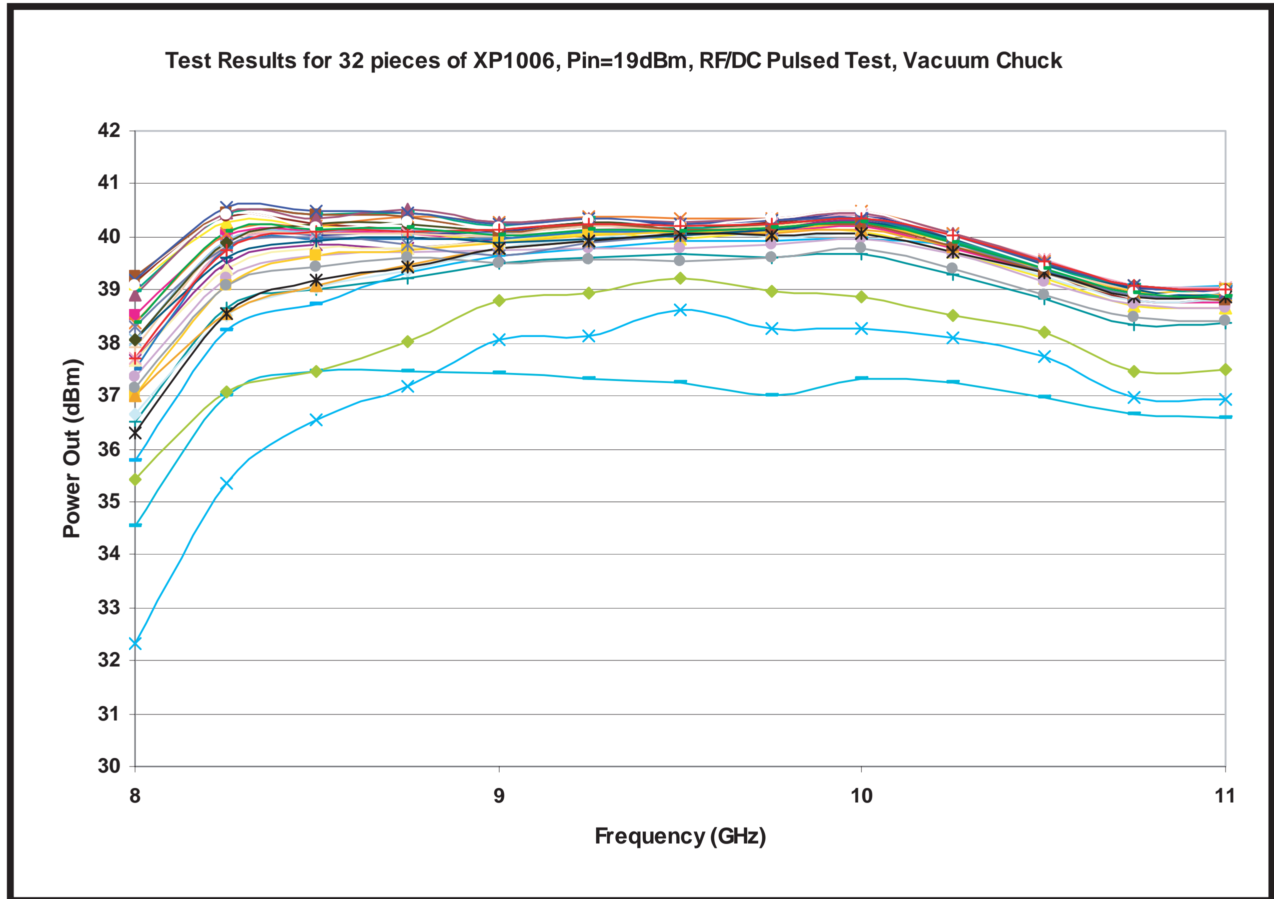

Figure 9: Sample of Test Results (on-wafer production test method

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(5) On-Wafer Test Validation

Since heating is potentially a problem with on-wafer testing, a sample of MMICs have undergone the same testing after they have been diced and soldered down to a large metal block (c.f. infinite heatsink). The results plotted in Figure 10 show that only a small difference in power level (due to thermal rise differences between a well heatsunk MMIC, and the same MMIC when tested on-wafer).

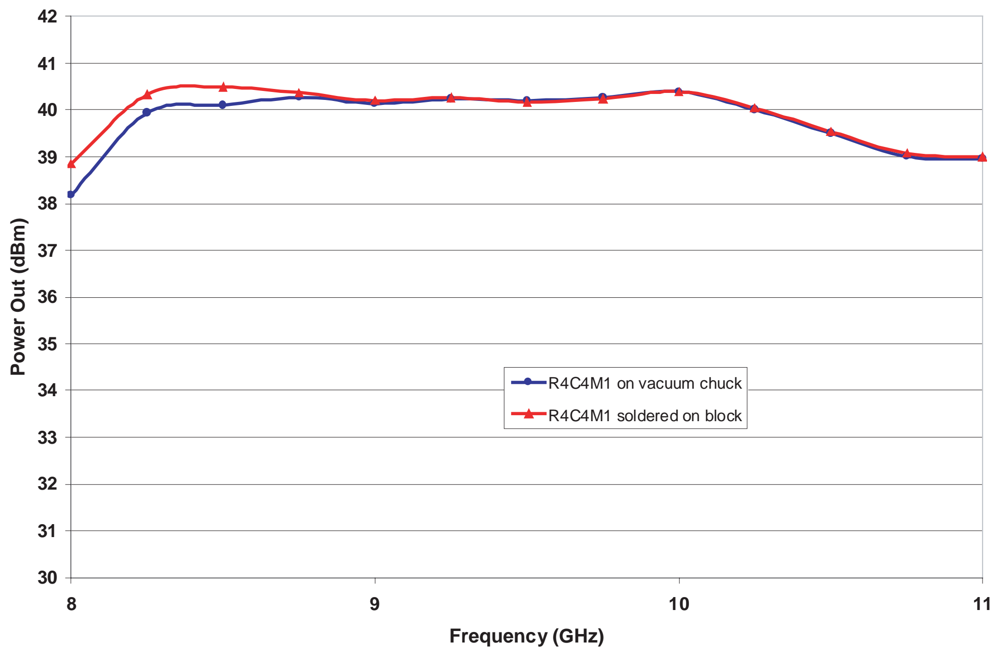

Figure 10: Comparison between an individual XP1006 tested on-wafer, and soldered down to a heatsink

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(6) XP1006 Troubleshooting

Following is a troubleshooting guideline if device failures or performance problems are being experienced with the XP1006 during evaluation.

During evaluation, if the XP1006 fails or performance is down, the most likely cause is that in the evaluation platform the MMIC is not stable. To check the stability, the following steps are recommended;

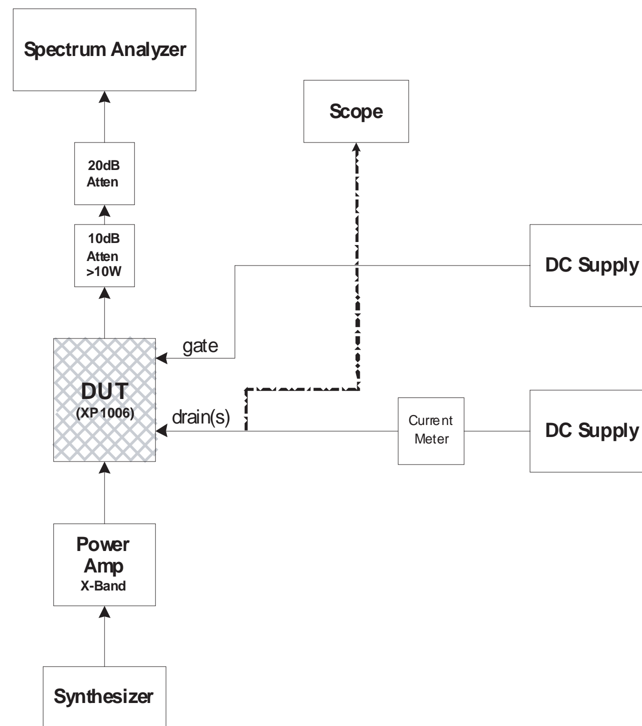

Figure 11: Basic CW-mode setup for Troubleshooting

CW check 1

(1) Before powering up the MMIC under evaluation, connect the evaluation platform to the test equipment as shown in Figure 11.
(2) The scope is used to check for oscillations on the drain lines.
(3) The spectrum analyzer should be set to a very wide span, and is used to check for in-band and/or out-of-band oscillations.
(4) The current meter is used for checking sudden increases in drain current, which indicates an oscillation is occurring. Note that the drain current will have small variations during the testing due to device heating.
(5) Set the gate voltage to -5V (must be applied before drain)
(6) Set the drain voltage to 2V
(7) Apply the desired RF input signal, and monitor all points.
(8) Gradually increase the drain voltage in 1V steps, up to 5V max. Check stability on all monitoring points while increasing the drain voltage.

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CW check 2

During CW check 1, if an oscillation occurs (or is thought to have occurred but not caught), do the following;

(1) re-bond the MMIC so that the gate line now goes to the gate pad on the south side of the MMIC (designated pin # 18 in the XP1006 data sheet). This will enable a linear increase in gate voltage to be applied.
(2) Set the gate voltage to -10V
(3) Set the drain voltage to 5V
(4) Slowly increase the gate voltage to -5V. Monitor all points for stability whilst increasing the gate current.
(5) The drain current measured should be smooth; a sudden increase indicates that at that point an oscillation has started.

Pulsed check

Once having verified that CW behavior is OK, pulsed stability checks can be done.

(1) Perform the same checks as those given in CW check 1 and CW check 2, but now in pulsed mode. Note the following;
    a. Because the MMIC is now tested in pulsed mode and will run cooler, the drain voltage can be swept from 2V to 8V in 1V steps (in CW it was 5V max due to heating)
    b. The drain current monitoring must now be made using a triggered output from the DC modulator (in CW, a standard current meter could be used).
    c. Using a conventional spectrum analyzer for monitoring oscillations will not be possible in this mode.
    d. The devices have been 100% tested with a DC pulse width of 5μs, an RF pulse width of 3μs, and a PRF of 10kHz. These parameters should be used in this check so performance can be directly compared.
    e. Ensure that there is adequate settling time between when the drain voltage is applied and when the RF pulse is applied. Production testing uses 2us delay.

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